UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/664,763	09/17/2003	Kent A. Dickey	10002827-2	1746

7590 01/24/2006

HEWLETT-PACKARD COMPANY
Intellectual Property Administration
P. O. Box 272400
Fort Collins, CO 80527-2400

EXAMINER	
MASKULINSKI, MICHAEL C	
ART UNIT	**PAPER NUMBER**
2113	

DATE MAILED: 01/24/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

UNITED STATES PATENT AND TRADEMARK OFFICE

Commissioner for Patents
United States Patent and Trademark Office
P.O. Box 1450
Alexandria, VA 22313-1450
www.uspto.gov

BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/664,763
Filing Date: September 17, 2003
Appellant(s): DICKEY ET AL.

R. Ross Viguet
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed November 28, 2005 appealing from the Office action mailed August 12, 2005.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings, which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

No evidence is relied upon by the examiner in the rejection of the claims under appeal.

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Double Patenting

Claims 21, 22, 23, 26, and 29-38 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-6 of U.S. Patent No. 6,651,193 B1.

Referring to claim 21, U.S. Patent 6,651,193 B1 discloses in claim 1 a distributed high performance coherent memory module with error containment, comprising:

a reading module for reading an error indication included in a packet reflective of a current state of a unit;

a determination module for determining if said state of a unit is in error mode;

a permission module for permitting a set of network traffic to operate in a normal state if said state of said unit is not in error mode;

a driving module for driving an error indicator to a subject processor if said state of said unit is in error mode;

a blocking module for ensuring that a set of corrupt traffic does not reach I/O devices if said current state of unit is in error mode;

a second reading module for ensuring that each member of a group of connected units reads said error indication included in said packet, if said state of said unit is in error mode;

a shared memory bit module therein for providing a shared memory bit within said error indication and further comprising a shared memory area within said unit;

and means for moving said error indication coextensive only with errors in particular data.

However, U.S. Patent 6,651,193 B1 discloses additional limitations not in claim 21, and U.S. Patent 6,651,193 B1 does not disclose a method for providing a distributed high performance coherent memory with full error containment. It would have been obvious to one of ordinary skill at the time of the invention to omit the limitations in U.S. Patent 6,651,193 B1 and to have a method for performing the same function as the apparatus in U.S. Patent 6,651,193 B1. A person of ordinary skill in the art would have been motivated to make the modifications because the omission of these limitations in claim 21 of the instant application is an obvious expedient since the remaining limitations in claim 1 of the U.S. Patent 6,651,193 B1 perform the same function as the limitations in claim 21 of the instant application (*In re Karlson*, 136 USPQ 184 (CCPA 1963)). Further, to have a method for performing the same function as the apparatus would be obvious because an apparatus is nothing more than a method being implemented.

Referring to claim 22, U.S. Patent 6,651,193 B1 discloses in claim 1 a second reading module for ensuring that each member of a group of connected units reads said error indication included in said packet, if said state of said unit is in error mode. However, U.S. Patent 6,651,193 B1 doesn't disclose a method step for ensuring that each member of a group of connected units reads said error indication included in said packet, if said state of said unit is in error mode. It would have been obvious to one of ordinary skill at the time of the invention to have a method for performing the same

function as the apparatus in U.S. Patent 6,651,193 B1. A person of ordinary skill in the art would have been motivated to make the modifications because to have a method for performing the same function as the apparatus would be obvious because an apparatus is nothing more than a method being implemented.

Referring to claim 23, U.S. Patent 6,651,193 B1 discloses in claim 2 a passing module for ensuring that each member of a group of connected units passes said error indication included in said packet, if said current state of a unit is in error mode, to a next unit member of group of connected units having at least one connected unit. However, U.S. Patent 6,651,193 B1 doesn't disclose a method step for ensuring that each member of said group of connected units having at least one connected unit passes said error indication included in said packet if said current state of a unit is in error mode to a next member of said group of connected units. It would have been obvious to one of ordinary skill at the time of the invention to have a method for performing the same function as the apparatus in U.S. Patent 6,651,193 B1. A person of ordinary skill in the art would have been motivated to make the modifications because to have a method for performing the same function as the apparatus would be obvious because an apparatus is nothing more than a method being implemented.

Referring to claim 26, U.S. Patent 6,651,193 B1 discloses in claim 4 a processor recovery module for implementing a recovery routine by said subject processor. However, U.S. Patent 6,651,193 B1 doesn't disclose a method step for implementing a recovery routine by said subject processor. It would have been obvious to one of ordinary skill at the time of the invention to have a method for performing the same

function as the apparatus in U.S. Patent 6,651,193 B1. A person of ordinary skill in the art would have been motivated to make the modifications because to have a method for performing the same function as the apparatus would be obvious because an apparatus is nothing more than a method being implemented.

Referring to claim 28, U.S. Patent 6,651,193 B1 discloses in claim 5 a unit recovery module for implementing a software recovery routine to clear said error mode from said unit. However, U.S. Patent 6,651,193 B1 doesn't disclose a method step for implementing a software recovery routine to clear said error mode. It would have been obvious to one of ordinary skill at the time of the invention to have a method for performing the same function as the apparatus in U.S. Patent 6,651,193 B1. A person of ordinary skill in the art would have been motivated to make the modifications because to have a method for performing the same function as the apparatus would be obvious because an apparatus is nothing more than a method being implemented.

Referring to claim 29, U.S. Patent 6,651,193 B1 discloses in claim 6 a shared memory error module for setting a shared memory error bit to be included in said packet for representing the presence of an error in a shared memory area. However, U.S. Patent 6,651,193 B1 doesn't disclose a method step for setting a shared memory error bit to be included in said packet as representative of a presence of an error in a shared memory area. It would have been obvious to one of ordinary skill at the time of the invention to have a method for performing the same function as the apparatus in U.S. Patent 6,651,193 B1. A person of ordinary skill in the art would have been motivated to make the modifications because to have a method for performing the same function as

the apparatus would be obvious because an apparatus is nothing more than a method being implemented.

Referring to claim 31, U.S. Patent 6,651,193 B1 discloses in claim 6 a shared memory error module for setting a shared memory error bit to be included in said packet for representing the presence of an error in a shared memory area. However, U.S. Patent 6,651,193 B1 doesn't disclose a method wherein said error bit is provided as a shared memory bit, and wherein said unit comprises a shared memory area. It would have been obvious to one of ordinary skill at the time of the invention to have a method for performing the same function as the apparatus in U.S. Patent 6,651,193 B1. A person of ordinary skill in the art would have been motivated to make the modifications because to have a method for performing the same function as the apparatus would be obvious because an apparatus is nothing more than a method being implemented.

Referring to claim 32, U.S. Patent 6,651,193 B1 discloses in claim 1 a distributed high performance coherent memory module with error containment, comprising:

a reading module for reading an error indication included in a packet reflective of a current state of a unit;

a determination module for determining if said state of a unit is in error mode;

a permission module for permitting a set of network traffic to operate in a normal state if said state of said unit is not in error mode;

a driving module for driving an error indicator to a subject processor if said state of said unit is in error mode;

a blocking module for ensuring that a set of corrupt traffic does not reach I/O devices if said current state of unit is in error mode;

a second reading module for ensuring that each member of a group of connected units reads said error indication included in said packet, if said state of said unit is in error mode;

a shared memory bit module therein for providing a shared memory bit within said error indication and further comprising a shared memory area within said unit;

and means for moving said error indication coextensive only with errors in particular data.

Although the conflicting claims are not identical, they are not patentably distinct from each other because claim 1 of U.S. Patent 6,651,193 B1 includes all of the limitations in claim 32 of the instant application. With regard to the additional limitations in claim 1 of U.S. Patent 6,651,193 B1, which are not included in claim 32 of the instant application, the omission of these limitations in claim 32 of the instant application is an obvious expedient since the remaining limitations in claim 1 of the U.S. Patent 6,651,193 B1 perform the same function as the limitations in claim 32 of the instant application (*In re Karlson*, 136 USPQ 184 (CCPA 1963)).

Referring to claims 33-37, U.S. Patent 6,651,193 B1 discloses the limitations of claims 33-37 in claims 2-6 respectfully. Although the conflicting claims are not identical, they are not patentably distinct from each other because claims 2-6 of U.S. Patent 6,651,193 B1 includes all of the limitations in claims 33-37 of the instant application. With regard to the additional limitations in claims 2-6 of U.S. Patent 6,651,193 B1, which

are not included in claims 33-37 of the instant application, the omission of these limitations in claims 33-37 of the instant application is an obvious expedient since the remaining limitations in claims 2-6, respectfully, of the U.S. Patent 6,651,193 B1 perform the same function as the limitations in claims 33-37, respectfully, of the instant application (*In re Karlson*, 136 USPQ 184 (CCPA 1963)).

Referring to claim 38, U.S. Patent 6,651,193 B1 in claim 1 discloses a shared memory bit module therein for providing a shared memory bit within said error indication and further comprising a shared memory area within said unit; and means for moving said error indication coextensive only with errors in particular data. Although the conflicting claims are not identical, they are not patentably distinct from each other because claim 1 of U.S. Patent 6,651,193 B1 includes all of the limitations in claim 38 of the instant application. With regard to the additional limitations in claim 1 of U.S. Patent 6,651,193 B1, which are not included in claim 38 of the instant application, the omission of these limitations in claim 38 of the instant application is an obvious expedient since the remaining limitations in claim 1 of U.S. Patent 6,651,193 B1 perform the same function as the limitations in claim 38 of the instant application (*In re Karlson*, 136 USPQ 184 (CCPA 1963)).

Claim Rejections - 35 USC § 102

Claims 21, 24-31, and 39 are rejected under 35 U.S.C. 102(e) as being anticipated by Gillett, Jr. et al., U.S. Patent 6,295,585 B1.

Referring to claim 21:

a. In the Abstract, Gillett, Jr. et al. disclose a multi-node computer network that includes a plurality of nodes coupled together via a data link. Each of the nodes includes a local memory, which further comprises a shared memory (high performance coherent memory).

b. In column 8, lines 50-55, Gillett, Jr. et al. disclose that when the Suppress Transmit After Error (STAE) bit is set, any write to the corresponding page of Memory Channel (MC) address space from a node that has detected an error at some point during the transaction of the data to another node in the network, will stop transmission once it has detected the error. And in column 8, lines 65-67 continued in column 9, lines 1-2, Gillett, Jr. et al. disclose that when the Suppress Receive After Error (SRAE) bit is set, if an error occurs during the receipt of a write to the page from the cluster, the MC adaptor at the receiving node will stop accepting data to the page for which this bit is set (reading an error indication included in a packet, reflective of a current state of a unit; determining if said current state of said unit is in error mode). Further, in column 13, lines 36-40, Gillett, Jr. et al. disclose that the STAE and SRAE bits are used in conjunction with the TPE and RPE bits, which are transmitted in the packet, to provide an error detection and recovery.

c. In column 8, lines 31-55, Gillett, Jr. et al. disclose that the system operates normally unless the STAE bit is set (permitting a network traffic set to operate in a normal state if said current state of a unit is not in error mode).

d. In column 8, lines 50-55, Gillett, Jr. et al. disclose that when the Suppress Transmit After Error (STAE) bit is set, any write to the corresponding page of Memory Channel (MC) address space from a node that has detected an error at some point during the transaction of the data to another node in the network, will stop transmission once it has detected the error (driving an error indicator to a subject processor if said current state of unit is in error mode).

e. In column 8, lines 50-55, Gillett, Jr. et al. disclose that when the Suppress Transmit After Error (STAE) bit is set, any write to the corresponding page of Memory Channel (MC) address space from a node that has detected an error at some point during the transaction of the data to another node in the network, will stop transmission once it has detected the error. Further, in column 14, lines 40-42, Gillett, Jr. et al. disclose that by halting data transmission from a faulty node, faulty data is not propagated to other nodes in the system (ensuring that corrupt traffic set does not reach an I/O device if said state of said unit is in error mode).

Referring to claim 24, in column 8, lines 50-55, Gillett, Jr. et al. disclose that when the Suppress Transmit After Error (STAE) bit is set, any write to the corresponding page of Memory Channel (MC) address space from a node that has detected an error at some point during the transaction of the data to another node in the network, will stop transmission once it has detected the error. And in column 8, lines 65-67 continued in column 9, lines 1-2, Gillett, Jr. et al. disclose that when the Suppress Receive After Error (SRAE) bit is set, if an error occurs during the receipt of a write to the page from the cluster, the MC adaptor at the receiving node will stop accepting data

to the page for which this bit is set (said error indication in said packet is in the form of an error bit).

Referring to claim 25, in column 9, lines 24-28, Gillett, Jr. et al. disclose that the MC header includes various information received from the page control table entry (said error indication in said packet contained within a header of said packet).

Referring to claims 26 and 28, in column 10, lines 25-29, Gillett, Jr. et al. disclose that the hardware provides certain basic structural elements that ensure adequate software control of the structure, such as guaranteeing that order on the data link is preserved, providing loop-back capability, and terminating transmission to facilitate quick handling of errors (implementing a software recovery routine by said subject processor).

Referring to claim 27, in column 8, lines 50-55, Gillett, Jr. et al. disclose that when the Suppress Transmit After Error (STAE) bit is set, any write to the corresponding page of Memory Channel (MC) address space from a node that has detected an error at some point during the transaction of the data to another node in the network, will stop transmission once it has detected the error. And in column 8, lines 65-67 continued in column 9, lines 1-2, Gillett, Jr. et al. disclose that when the Suppress Receive After Error (SRAE) bit is set, if an error occurs during the receipt of a write to the page from the cluster, the MC adaptor at the receiving node will stop accepting data to the page for which this bit is set (said reading step includes reading said error indication from an error bit).

Referring to claims 29 and 31, in the Abstract, Gillett, Jr. et al. disclose a multi-node computer network that includes a plurality of nodes coupled together via a data link. Each of the nodes includes a local memory, which further comprises a shared memory. Further, in column 8, lines 50-55, Gillett, Jr. et al. disclose that when the Suppress Transmit After Error (STAE) bit is set, any write to the corresponding page of Memory Channel (MC) address space from a node that has detected an error at some point during the transaction of the data to another node in the network, will stop transmission once it has detected the error. And in column 8, lines 65-67 continued in column 9, lines 1-2, Gillett, Jr. et al. disclose that when the Suppress Receive After Error (SRAE) bit is set, if an error occurs during the receipt of a write to the page from the cluster, the MC adaptor at the receiving node will stop accepting data to the page for which this bit is set. Thus the error bit that is set is in response to an error in shared memory (setting a shared memory error bit to be included in said packet as representative of a presence of an error in a shared memory area).

Referring to claim 30, in column 8, lines 50-55, Gillett, Jr. et al. disclose that when the Suppress Transmit After Error (STAE) bit is set, any write to the corresponding page of Memory Channel (MC) address space from a node that has detected an error at some point during the transaction of the data to another node in the network, will stop transmission once it has detected the error. And in column 8, lines 65-67 continued in column 9, lines 1-2, Gillett, Jr. et al. disclose that when the Suppress Receive After Error (SRAE) bit is set, if an error occurs during the receipt of a write to

the page from the cluster, the MC adaptor at the receiving node will stop accepting data to the page for which this bit is set (said error bit is provided as a fatal error bit).

Referring to claim 39, in column 9, lines 24-28, Gillett, Jr. et al. disclose that the MC header includes various information received from the page control table entry (means for transporting error indications together with data which is in error). Further, in Figure 8, Gillett, Jr. et al. disclose that the header is sent with the data. In column 8, lines 50-55, Gillett, Jr. et al. disclose that when the Suppress Transmit After Error (STAE) bit is set, any write to the corresponding page of Memory Channel (MC) address space from a node that has detected an error at some point during the transaction of the data to another node in the network, will stop transmission once it has detected the error. And in column 8, lines 65-67 continued in column 9, lines 1-2, Gillett, Jr. et al. disclose that when the Suppress Receive After Error (SRAE) bit is set, if an error occurs during the receipt of a write to the page from the cluster, the MC adaptor at the receiving node will stop accepting data to the page for which this bit is set (means at each device to which such error data is directed and controlled in part by said error indicators for containing within said device said error data). Further, in column 13, lines 36-40, Gillett, Jr. et al. disclose that the STAE and SRAE bits are used in conjunction with the TPE and RPE bits, which are transmitted in the packet, to provide an error detection and recovery.

(10) Response to Argument

On page 5, with respect to claim 21, the Appellant argues, "Claim 21 defines a method for providing a distributed high performance coherent memory with error

containment that includes reading an error indication included in a data packet, reflective of a current state of a unit. Gillett does not disclose at least this limitation."

The Examiner respectfully disagrees and believes that the Appellant doesn't fully understand the Examiner's Final Office Action or has chosen not to read it. So for Appellant's edification, the Examiner submits the following, which was submitted in the Final Office Action:

A distributed high performance coherent memory with error containment	See Abstract of Gillett, Jr. et al.
Reading an error indication included in a data packet, reflective of a current state of a unit and determining if said current state of said unit is in error mode	See column 8, lines 50-55, column 8, lines 65-67 continued in column 9, lines 1-2, and column 13, lines 36-40 of Gillett, Jr. et al. (explicitly discloses TPE and RPE bits transmitted in the packet used in conjunction with the STAE and SRAE bits)
Permitting a network traffic set to operate in a normal state if said current state of a unit is not in error mode	See column 8, lines 31-55 of Gillett, Jr. et al.
Driving an error indicator to a subject processor if said current state of unit is in error mode	See column 8, lines 50-55 of Gillett, Jr. et al.
Ensuring that corrupt traffic set does not	See column 8, lines 50-55, column 14,

reach an I/O device if said state of said unit is in error mode	lines 40-42 of Gillett, Jr. et al.

Further, in column 12, lines 7-10, Gillett, Jr. et al. disclose that the mechanism for ensuring reliable data delivery makes use of the ACK field in the header portion of the MC packet to provide an MC ACK transaction. In column 12, lines 30-48, Gillett, Jr. et al. disclose that the MC ACK Response is a returned byte of data, which contains MC error summary information. The Valid bit is used to indicate that the responding node received the packet of data. The TPE bit is used to indicate whether there was a Transmit Path Error, that is an error on the transmit portion of a previous MC transaction. The RPE bit is used to indicate whether there was a Receive Path error, i.e. an error on the receive portion of a previous MC transaction. In column 13, lines 36-40, Gillett, Jr. et al. disclose that the STAE and SRAE bits are used in conjunction with the TPE and RPE bits, which are transmitted in the packet, to provide an error detection and recovery. Further, in column 13, lines 41-51 and in column 13 line 66 through column 14 line 7, Gillett discloses that the TPE bit and RPE bit indicates errors in the unit.

On page 5, with respect to claim 32, the Appellant's argument is unnecessary since the only outstanding rejection on claim 32 is a double patenting rejection. The Examiner has indicated in the previous Office Action that this claim would be allowable if the double patenting rejection was overcome. Therefore, the Examiner will disregard the argument of claim 32.

On page 5, with reference to claim 39, the Appellant argues, "Claim 39 defines a system for error containment comprising means for transporting error indications together with data which is in error. Gillett does not disclose at least this limitation." The Examiner respectfully disagrees and believes that the Appellant doesn't fully understand the Examiner's Final Office Action or has chosen not to read it. So for Appellant's edification, the Examiner submits the following, which was submitted in the Final Office Action:

Means for transporting error indications together with data which is in error	See column 9, lines 24-28, Gillett, Jr. et al.
Means at each device to which such error data is directed and controlled in part by said error indicators for containing within said device said error data	See Figure 8, column 8, lines 50-55, column 8, lines 65-67 continued in column 9, lines 1-2, and column 13, lines 36-40 of Gillett, Jr. et al.

Further, in column 12, lines 7-10, Gillett, Jr. et al. disclose that the mechanism for ensuring reliable data delivery makes use of the ACK field in the header portion of the MC packet to provide an MC ACK transaction. In column 12, lines 30-48, Gillett, Jr. et al. disclose that the MC ACK Response is a returned byte of data, which contains MC error summary information. The Valid bit is used to indicate that the responding node received the packet of data. The TPE bit is used to indicate whether there was a Transmit Path Error, that is an error on the transmit portion of a previous MC transaction. The RPE bit is used to indicate whether there was a Receive Path error,

i.e. an error on the receive portion of a previous MC transaction. In column 13, lines 36-40, Gillett, Jr. et al. disclose that the STAE and SRAE bits are used in conjunction with the TPE and RPE bits, which are transmitted in the packet, to provide an error detection and recovery. Further, in column 13, lines 41-51 and in column 13 line 66 through column 14 line 7, Gillett discloses that the TPE bit and RPE bit indicates errors in the unit.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

MM

Conferees:

Robert Beausoliel

SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100

Robert Beausoliel

Lynne Browne

LYNNE H. BROWNE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100